REMARKS

In the Office Action, the Examiner rejected Claims 1-6 and 10-18 over the prior art. Also, the Examiner objected to Claims 7-9 as being dependent upon a rejected base claim, and indicated that these claims would be allowable if appropriately rewritten. In addition, the Examiner objected to the specification, to the drawings, and to some of the language in the claims.

With respect to the rejection of the claims over the prior art, Claims 1, 3-6, 10, 12-14 and 16-18 were rejected under 35 U.S.C. §102 as being fully anticipated by an IEEE paper "A Systemic Approach to SER Estimation and Solutions" (Nguyen, et al.). Claims 2, 11 and 15 were rejected under 35 U.S.C. §103 as being unpatentable over Nguyen, et al. in view of a second IEEE paper "Analyzing Soft Errors In Leakage Optimized SRAM Design" (Degalahal, et al.).

For the reasons discussed below, the rejections of Claims 1-6 and 10-18 over the prior art are respectfully traversed. Claims 7 and 9 are herein being rewritten in independent form to put these claims, and Claim 8, in condition for allowance. Also, the specification, drawings and the language of Claims 1, 10 and 14 are being rephrased in view of the Examiner's objections. Claim 19, which is dependent from Claim 1, is being added to describe preferred features of the invention.

In response to the Examiner's objection to the specification, this opportunity is being taken to correct informalities in paragraph 15 and 25, as suggested by the Examiner. It is believed that this corrects all the informalities in the specification, and the Examiner is, accordingly, asked to reconsider and to withdraw the objection to the specification. If the

IN THE DRAWINGS:

Applicants ask permission to label Figures 1-3 as "Prior Art", as shown on the attached Replacement and Annotated Sheets.

Examiner believes that additional corrections are needed, the Examiner is requested to telephone the undersigned.

The Examiner objected to the drawings on the grounds that Figures 1-3 should be labeled as "Prior Art." Applicants are herewith submitting formal drawings for this application. It is noted that, in these formal drawings, Figures 1-3 are labeled "Prior Art," and the Examiner is thus also requested to reconsider and to withdraw the objection to the drawings.

In objecting to the language of the claims, the Examiner suggested amending Claim 1, line 3, Claim 10, line 2, and claim 14, line 4 to change "the circuit" to "the circuits included in the integrated circuit." These claims are herein being amended in this way.

The Examiner also asked that the beginning of the preambles of the dependent claims be changed from "A" method, system, or program, to "The" method, system or program. Applicants respectfully request that this objection be withdrawn. The use of "A" to introduce the claims emphasizes that there are many specific types of methods, systems, or programs that come within the scope of the claims. The use of the word "A" is appropriate and acceptable.

In view of the foregoing changes and discussion, the Examiner is respectfully asked to reconsider and to withdraw the objections to the specification, the drawings and the language of the claims.

With regard to the claims, Claims 7 and 9 are being rewritten in independent form including all of the limitations of Claims 1 and 6. This places Claim 7, Claim 8, which is dependent from Claim 7, and Claim 9 in condition for allowance without further argument.

The Examiner is thus also asked to reconsider and to withdraw the objections to Claims 7-9, and to allow these claims.

The rejections of Claims 1-6 and 10-18 over the prior art are respectively traversed because the cited references do not disclose or suggest the combination of the timing and soft error analysis described in independent Claims 1, 10 and 14. In particular, it is noted that Nguyen, et al. do not take timing into account in their analysis.

In order to best understand this, it may be helpful if Applicants briefly discuss the invention and the prior art.

The present invention, generally, relates to a method and system for reducing the failure rates of nets of an integrated circuit due to soft errors without impacting the timing on critical paths of the circuit. To do this, the present invention performs a timing analysis of the circuits to ensure that they meet specified timing criteria, and performs soft error analysis of the circuits to determine whether they meet specified soft error criteria. Those circuits that fail the soft error analysis are improved to improve their resistance to soft errors.

Nguyen, et al. discloses a procedure for estimating a soft error rate. The paper finds that latches/flip-flops and combinational logic contribute significantly to the overall chip failure in time rate.

Degalahal, et al. describes a process for analyzing soft errors in a SRAM design. The paper contends that there is a trade off between optimizing the leakage power and improving the immunity to soft errors.

While it is true that Nguyen, et al and Degalahal, et al do give an approach for estimation of soft error rate (SER), they do not disclose the unique and new claims of the present application. In particular, they do not take timing into account in their analysis.

Independent Claims 1, 10 and 14 describe this feature of the invention. In particular, claims 1 and 14 positively set forth the steps of performing a timing analysis of the circuits to ensure that they meet specified timing criteria, and performing soft error analysis of the circuits to determine whether they meet specified soft error criteria. These claims also set forth the step of improving those circuits that fail the soft error analysis to improve their resistance to soft errors. Claim 10, which is directed to a system for simulating an integrated circuit, describes analogous apparatus features.

The other references of record have been reviewed, and these other references, whether they are considered individually or in combination, also do not disclose or suggest the above-described combination of analysis.

Because of the above-described differences between Claims 1, 10 and 14, and because of the advantages associated with those differences, these claims patentably distinguish over the prior art and are allowable. Claims 2-6, and 19 are dependent from Claim 1 and are allowable therewith. Similarly, Claims 11-13 are dependent from, and are allowable with, Claim 10; and Claims 15-18 are dependent from Claim 14 and are allowable therewith.

In addition to the foregoing, there are important additional feature of the invention described in the dependent claims that also are not taught by the prior art.

For example, Claims 3 and 12 do not simply present the algorithm of calculating the failure rate, but a more complete methodology for including SER improvement without impacting timing. These claims are not directed to the method for failure rate due to SER as Nguyen, et al. present.

Claims 4, 13 and 16 are unique. After fixing a circuit for SER, one must retime to make sure the circuit is still fast enough. This is not discussed anywhere within Nguyen, et al.

Claims 5, 6, 17 and 18 should not be rejected. These claims show the iterative portions of the methodology described within this application and are not mentioned in Nguyen, et al.

With particular regard to the Examiner's rejection of Claims 2, 11 and 15 over the combination of Nguyen, et al. and Degalahal, et al, it may be helpful to note that these claims are not directed merely to the use of raising VDD. What is important is that the timing net gets a voltage boost or some other SER improvement. The methodology is varied according to the timing net as a step within the overall flow of the methodology. Moreover, these claims are not directed, generally, to increasing Qcrit by raising VDD or adding capacitance. Instead, these claims are directed to the methodology of finding which timing critical nets get a VDD boost and which non-timing critical nets can have either a VDD boost or added capacitance.

In view of the foregoing, it is believed that Claims 1-6 and 10-19 patentably distinguish over the prior art and are allowable. The Examiner is, accordingly, asked to reconsider and to withdraw the rejection of Claims 1, 3-6, 10, 12-14 and 16-18 under 35 U.S.C. §102 and the rejection of Claims 2, 11 and 15 under 35 U.S.C. §103, and to allow Claims 1-6 and 10-19.

For the reasons discussed above, the Examiner is respectfully requested to reconsider and to withdraw the objections to the specification, the drawings, and the language of the claims. The Examiner is further asked to reconsider and to withdraw the rejections of Claims 1-6 and 10-18 and the objection to Claims 7-9, and to allow Claims 1-19. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,

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Enclosures (Two Annotated Sheet and Two Replacement Sheets for Figures 1, 2 and 3)

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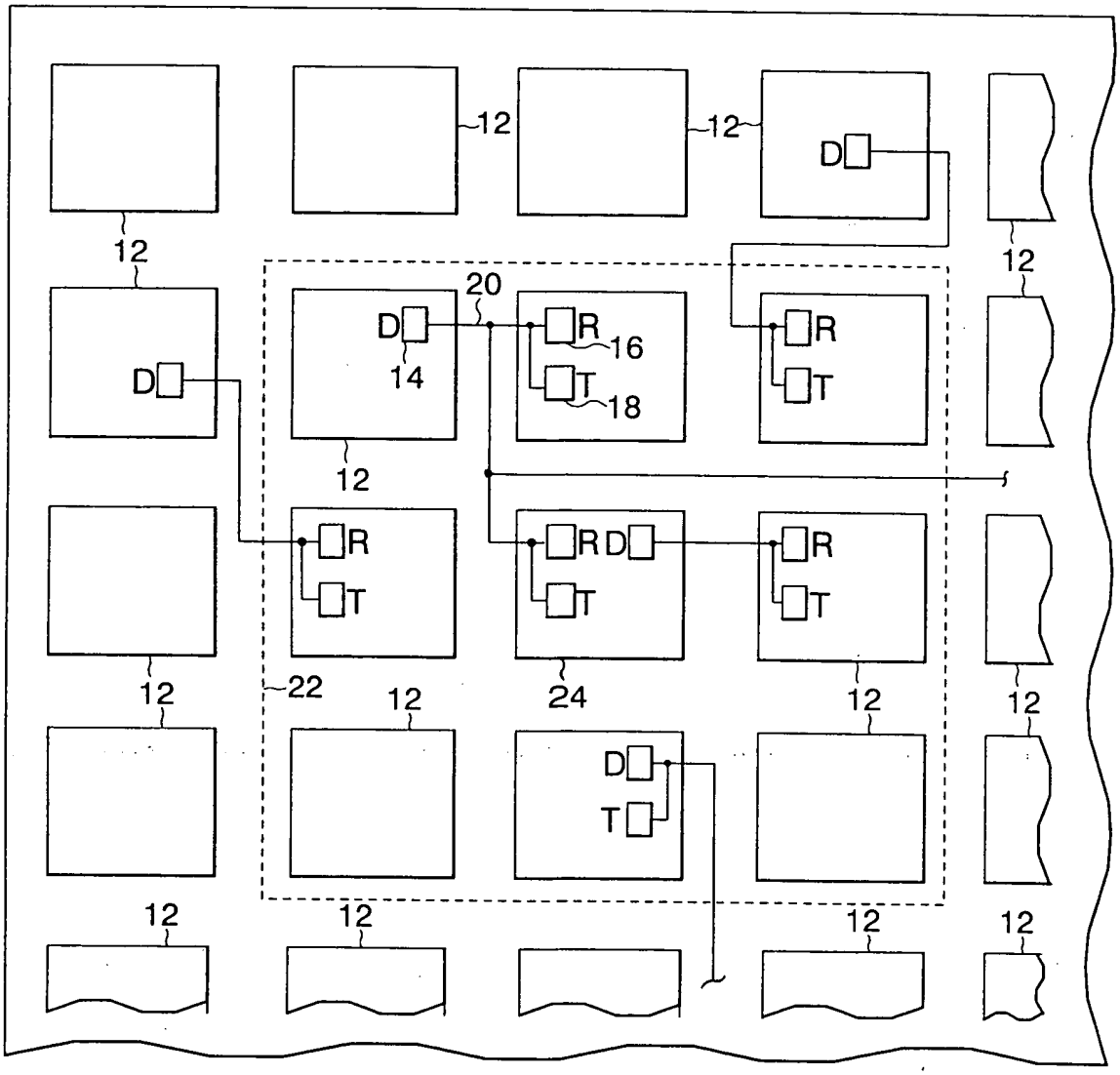
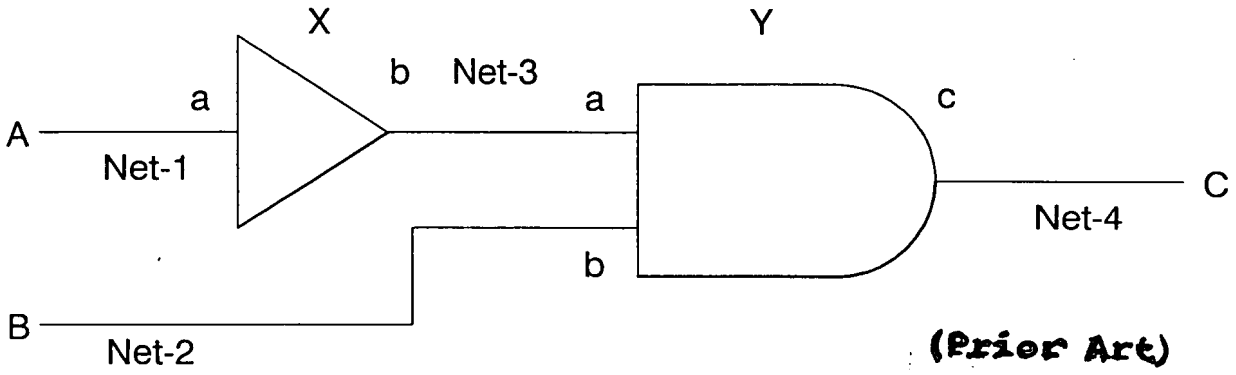


(Prior Art)

Figure 1



EXAMPLE OF LOGIC CIRCUIT

Figure 2

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Port:
  INPUT : A, B:
  OUTPUT: C
EndPort
Net:
  Net-1: pA, Xpa;
  Net-2: pB, Ypb;
  Net-3: Xpb, Ypa;
  Net-4; pC, Ypc;
EndNet;
```

(Prior Art)

EXAMPLE OF NET LIST

Figure 3